

## DESCRIPTION

The MP4021 is a primary-side-control offline LED lighting controller that achieves high power factor and accurate LED current for isolated single-power-stage lighting applications in a single SOIC8 package. The proprietary real-current control method accurately controls LED current from primary-side information. Eliminating the secondary-side feedback components and the optocoupler significantly simplifies the LED lighting system design.

The MP4021 integrates power factor correction and works in boundary conduction mode to reduce the MOSFET switching losses.

The extremely low start-up current and quiescent current reduces the total power consumption and provides a high-efficiency solution for lighting applications.

The multi-protection features of MP4021 greatly enhance system reliability and safety. The MP4021 features over-voltage protection, short-circuit protection, cycle-by-cycle current limiting, V<sub>CC</sub> UVLO, and auto-restart over-temperature protection.

## FEATURES

- Real current control without secondary-feedback circuit
- Unique architecture for superior line regulation
- High power factor  $\geq 0.9$  over universal input voltage
- Boundary conduction mode improves efficiency
- Ultra-low (20 $\mu$ A) start-up current
- Low (1mA) quiescent current
- Input UVLO
- Cycle-by-cycle current limit
- Over-voltage protection
- Short-circuit protection
- Over-temperature protection
- Available in an SOIC8 package

## APPLICATIONS

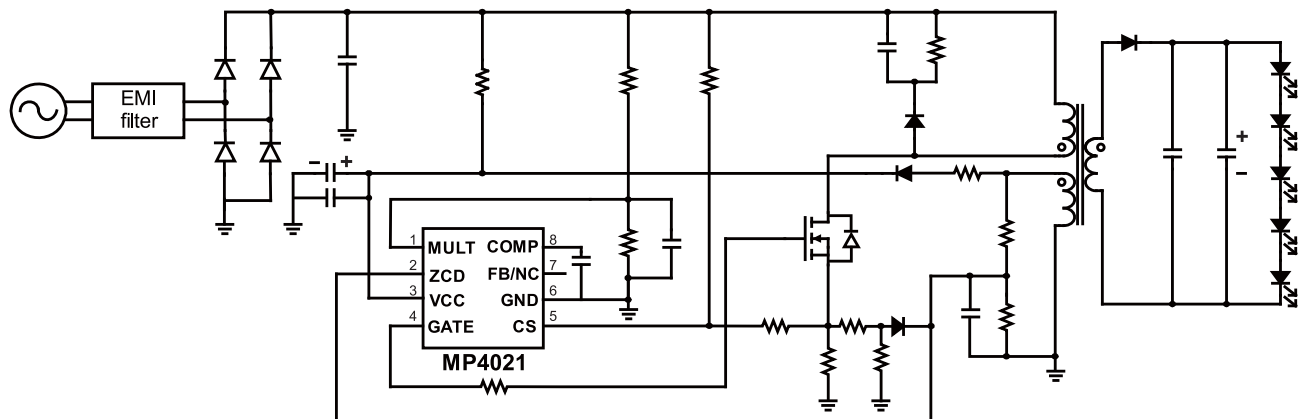
- Solid-state lighting
- Industrial and commercial lighting
- Residential lighting

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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The MP4021 is under patent pending.

## TYPICAL APPLICATION

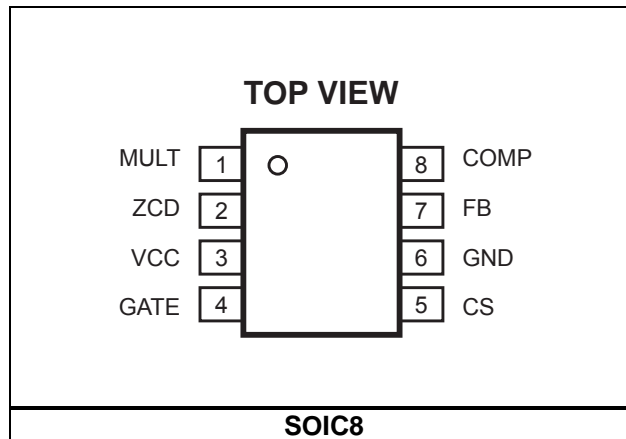


### ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4021GS	SOIC8	MP4021

\* For Tape & Reel, add suffix -Z (e.g. MP4021GS-Z);

### PACKAGE REFERENCE



#### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Input Voltage $V_{CC}$ .....	-0.3V to +30V
ZCD Pin .....	-7V to +7V
Other Analog Inputs and Outputs .....	-0.3V to 7V
Max. Gate Current .....	$\pm 1.2A$
Continuous Power Dissipation ( $T_A = +25^\circ C$ ) <sup>(2)</sup>	
SOIC8 .....	1.3W
Junction Temperature .....	150°C
Lead Temperature .....	260°C
Storage Temperature .....	-65°C to +150°C

#### Recommended Operating Conditions <sup>(3)</sup>

Supply Voltage $V_{CC}$ .....	10.3V to 23V
Maximum Junction Temp. ( $T_J$ ) .....	+125°C

#### Thermal Resistance <sup>(4)</sup>

	$\theta_{JA}$	$\theta_{JC}$
SOIC8 .....	96	45 ... °C/W

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J(MAX)$ , the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D(MAX) = (T_J(MAX) - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operation conditions.
- Measured on JESD51-7 4-layer board.

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 14V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Supply Voltage</b>						
Operating Range	$V_{CC}$	After turn on	10.3		23	V
Turn-on Threshold	$V_{CC\_ON}$	$V_{CC}$ rising edge	12.6	13.6	14.6	V
Turn-off Threshold	$V_{CC\_OFF}$	$V_{CC}$ falling edge	8.4	9.0	9.6	V
Hysteretic Voltage	$V_{CC\_HYS}$			4.5		V
<b>Supply Current</b>						
Start-up Current	$I_{STARTUP}$	$V_{CC}=11V$		20	30	$\mu A$
Quiescent Current	$I_Q$	No switching		0.75	1	mA
Operating Current	$I_{CC}$	$F_s = 70kHz$		2	3	mA
<b>Multiplier</b>						
Operation Range	$V_{MULT}$		0		3	V
Gain	$K^{(5)}$			1		1/V
<b>Error Amplifier</b>						
Feedback Voltage	$V_{FB}$		0.403	0.414	0.425	V
Transconductance <sup>(6)</sup>	$G_{EA}$			222		$\mu A/V$
Upper Clamp Voltage	$V_{COMP\_H}$		5.3	5.65	6	V
Lower Clamp Voltage	$V_{COMP\_L}$		1.3	1.5	1.7	V
Max Source Current <sup>(6)</sup>	$I_{COMP}$			75		$\mu A$
Max Sink Current <sup>(6)</sup>	$I_{COMP}$			-400		$\mu A$
<b>Current Sense Comparator</b>						
Leading Edge Blanking Time	$t_{LEB}$			280		ns
Current Sense Clamp Voltage	$V_{CS\_CLAMP}$		2.3	2.5	2.7	V
<b>Zero Current Detector</b>						
Zero Current Detect threshold	$V_{ZCD\_T}$	$V_{ZCD}$ falling edge		0.31		V
Zero Current Detect Hysteresis	$V_{ZCD\_HYS}$			650		mV
ZCD Blanking Time	$t_{LEB\_ZCD}$	After turn-off	1.8	2.5	3.2	$\mu s$
Over-voltage Blanking Time	$t_{LEB\_OVP}$	After turn-off		1.5		$\mu s$
Over-voltage Threshold	$V_{ZCD\_OVP}$	1.5 $\mu s$ delay after turn-off	5.1	5.4	5.7	V
Over-current Blanking Time	$t_{LEB\_OCP}$	After turn-on, same as $t_{LEB}$		280		ns
Over-current Threshold	$V_{ZCD\_OCP}$	280ns delay after turn-on	0.57	0.60	0.63	V
Minimum Off Time	$t_{OFF\_MIN}$		2	3.5	5	$\mu s$
<b>Starter</b>						
Start Timer Period	$t_{START}$			130		$\mu s$

**ELECTRICAL CHARACTERISTICS** (Continued) $V_{CC} = 14V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Gate Driver</b>						
Output Clamp Voltage	$V_{GATE\_CLAMP}$	$V_{CC}=23V$	12	13.5	15	V
Minimum Output Voltage	$V_{GATE\_MIN}$	$V_{CC}=V_{CC\_OFF} + 50mV$	6.0			V
Max Source Current <sup>(6)</sup>	$I_{GATE\_SOURCE}$			1		A
Max Sink Current <sup>(6)</sup>	$I_{GATE\_SINK}$			-1.2		A

**Notes:**5) The multiplier output is given by:  $V_{CS}=K \cdot V_{MULT} \cdot (V_{COMP}-1.5)$ 

6) Guaranteed by design.

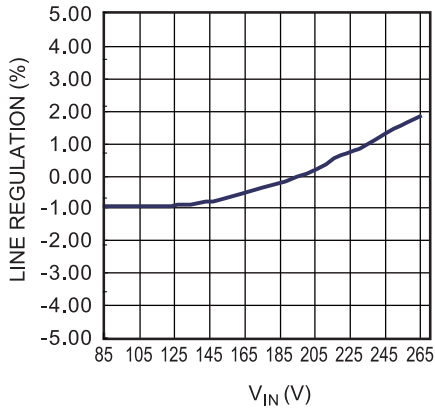
## PIN FUNCTIONS

Pin #	Name	Pin Function
1	MULT	Multiplier input. Connect this pin to the tap of resistor divider from the rectified voltage of the AC line. The half-wave sinusoid signal to this pin provides a reference signal for the internal current control loop.
2	ZCD	Zero-current detection. A negative going-edge triggers the turn-on signal of the external MOSFET. Connect this pin to a resistor divider between the auxiliary winding to GND. Over-voltage condition is detected through ZCD. Every switching turn-off interval, if ZCD voltage is higher than the over-voltage-protection (OVP) threshold after the 1.5 $\mu$ s blanking time, the over-voltage protection will trigger and the system will stop switching until auto-restart comes. ZCD pin can also monitor over-current condition. Connect this pin thru a diode to a resistor divider between CS to GND. Every switching turn-on interval, if ZCD voltage is higher than the over-current-protection (OCP) threshold after the 280ns blanking time, the over-current protection will trigger and the system will stop switching until auto-restart comes.
3	VCC	Power supply input. This pin supplies the power for the control signal and the high-current MOSFET grade drive output. Bypass this pin to ground with an external bulk capacitor of typically 22 $\mu$ F in parallel with a 100pF ceramic cap to reduce noise.
4	GATE	Gate drive output. This totem pole output stage is able to drive a high-power MOSFET with a peak current of 1A source capability and 1.2A sink capability. The high level voltage of this pin is clamped to 13.5V to avoid excessive gate drive voltage. And the low level voltage is higher than 6V to guarantee enough drive capacity.
5	CS	Current sense. The MOSFET current is sensed via a sensing resistor to its source lead. The comparison between the resulting voltage and the internal sinusoidal-current reference signal determines when the MOSFET turns off. A feed-forward from the rectified AC line voltage connected to the current sense pin maximizes the line regulation. If the pin voltage is higher than the current limit threshold of 2.5V (after turn-on blanking) the gate drive will turn off.
6	GND	Ground. Current return for the control signal and the gate drive signal.
7	FB/NC	Feedback signal. Leave this pin floating (NC) for primary-side control.
8	COMP	Loop compensation input. Connect a compensation network to stabilize the LED drive and maintain an accurate LED current.

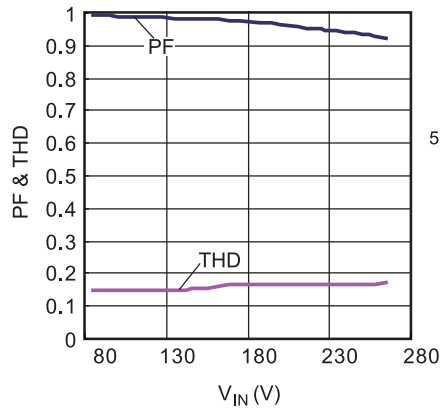
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 110V_{AC}/220V_{AC}$ , 5 LEDs in series,  $I_{LED} = 500mA$ ,  $L_m = 2.2mH$ ,  $N_p:N_s:N_{AUX} = 144:24:27$ , unless otherwise noted.

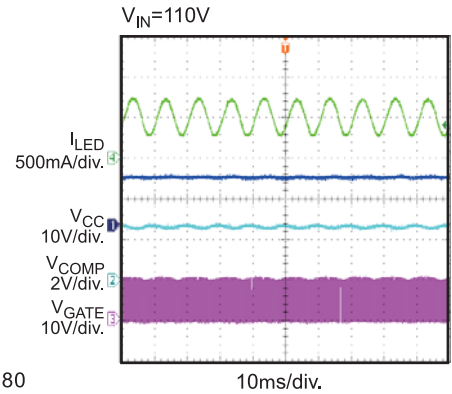
**Line Regulation**



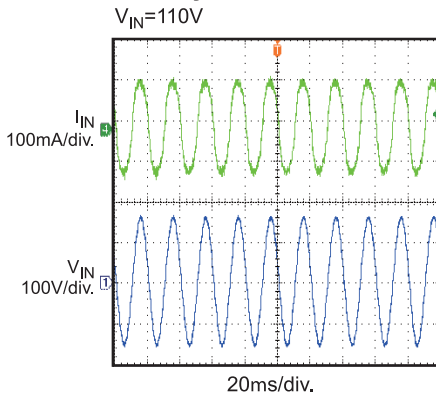
**PF & THD vs.  $V_{IN}$**



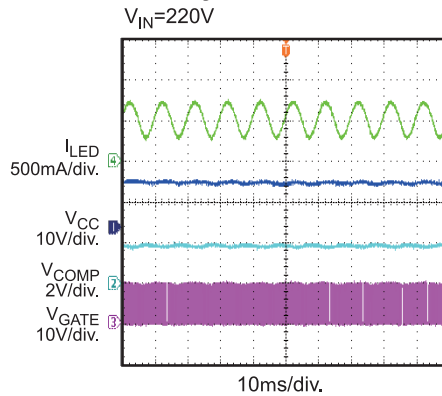
**Steady State**



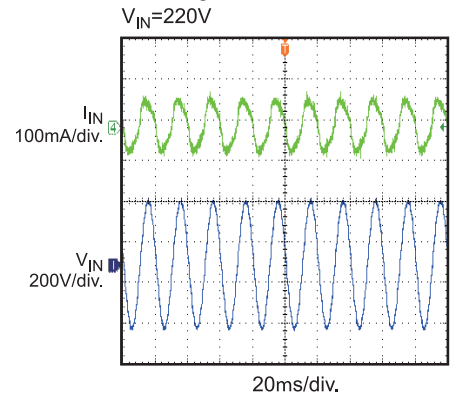
**Steady State**



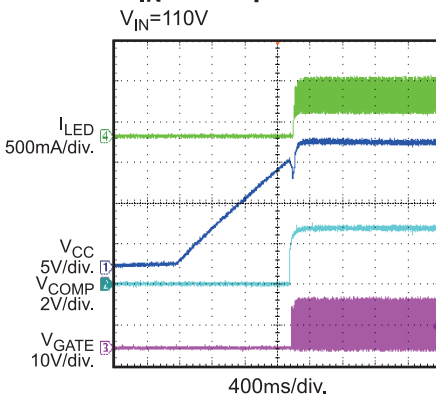
**Steady State**



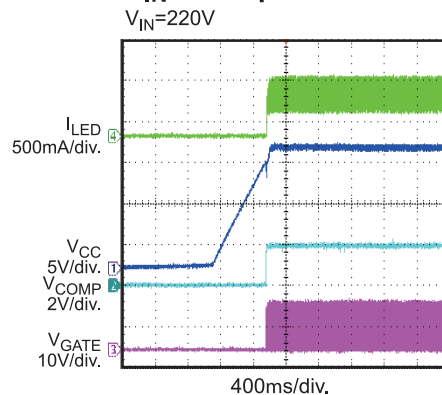
**Steady State**



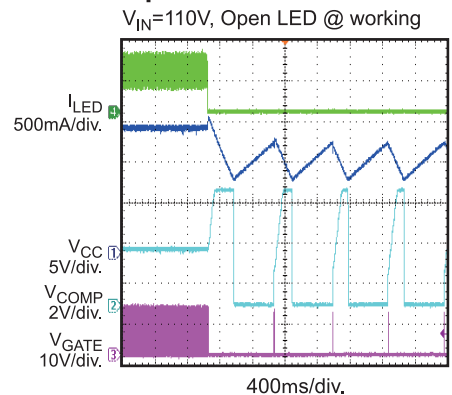
**$V_{IN}$  Startup**



**$V_{IN}$  Startup**



**Open LED Protection**

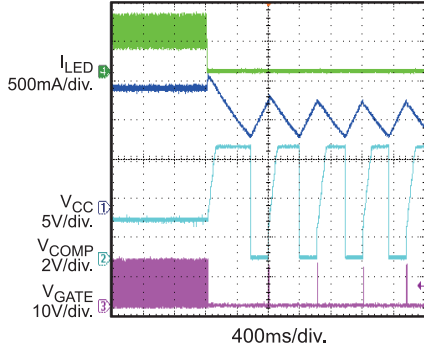


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

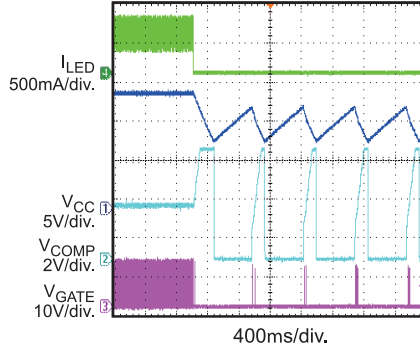
$V_{IN} = 110V_{AC}/220V_{AC}$ , 5 LEDs in series,  $I_{LED} = 500mA$ ,  $L_m = 2.2mH$ ,  $N_p:N_s:N_{AUX} = 144:24:27$ , unless otherwise noted.

**Open LED Protection**

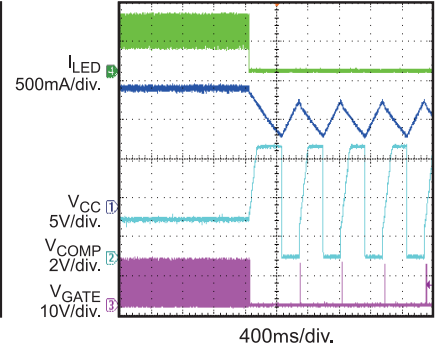
$V_{IN} = 220V$ , Open LED @ working


**Short Circuit Protection**

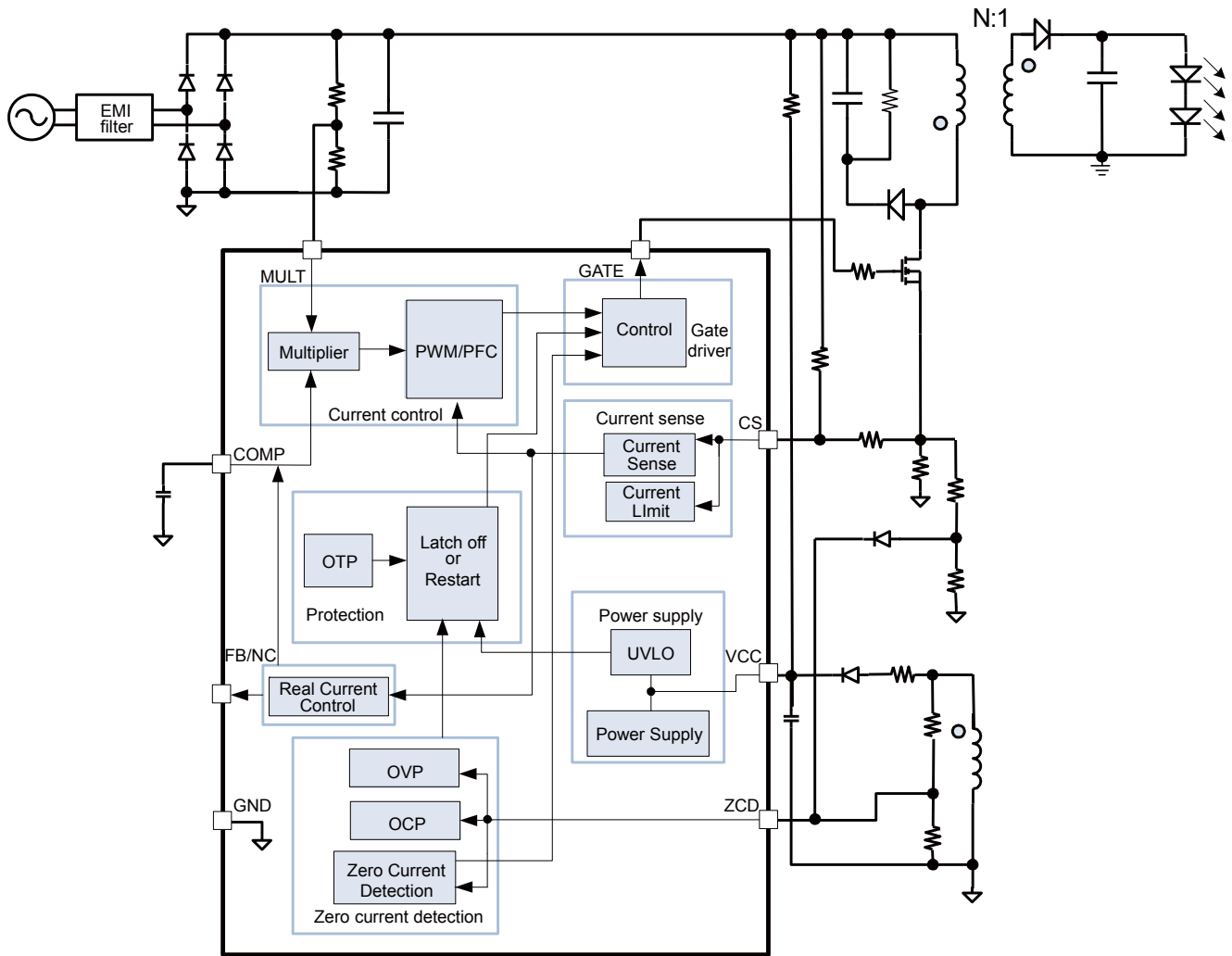
$V_{IN} = 110V$ , Short LED+ to LED- @ working


**Short Circuit Protection**

$V_{IN} = 220V$ , Short LED+ to LED- @ working



**FUNCTION DIAGRAM**



**Figure 1—MP4021 Function Block Diagram**



## OPERATION

The MP4021 is a primary-side control offline LED controller which incorporates all the features for high-performance LED lighting. The LED current can be accurately controlled with the real current control method from the primary-side information. Active Power Factor Correction (PFC) eliminates unwanted harmonic noise to pollute the AC line.

### Start Up

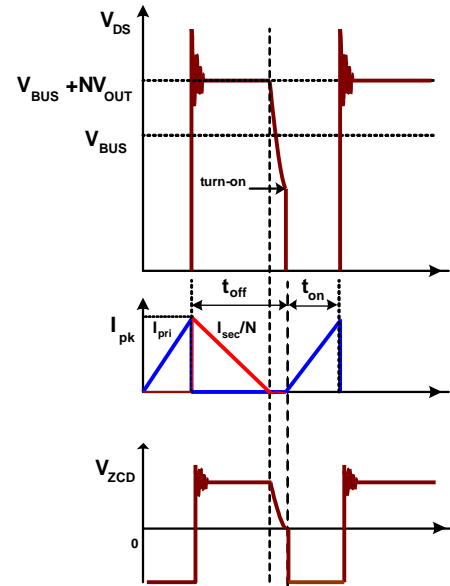
Initially, VCC of the MP4021 is charged through the start up resistor from the AC line. When VCC reaches 13.6V, the control logic works and the gate drive signal begins to switch. Then the power supply is taken over by the auxiliary winding.

The MP4021 will shut down when VCC drops below 9V.

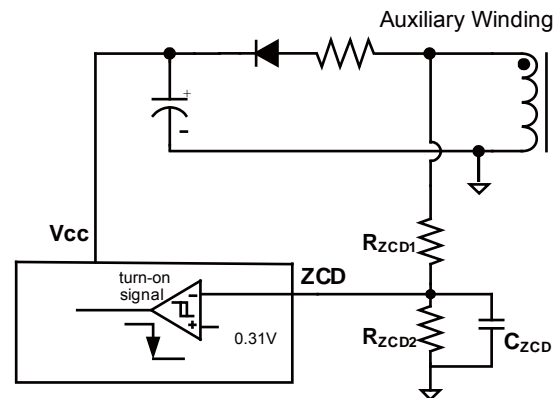
### Boundary Conduction Mode Operation

During the external MOSFET on time ( $t_{ON}$ ), the rectified input voltage ( $V_{BUS}$ ) applies to the primary-side inductor ( $L_m$ ), and the primary current ( $I_{pri}$ ) increases linearly from zero to the peak value ( $I_{pk}$ ). When the external MOSFET turns off, the energy stored in the inductor is transferred to the secondary-side and turns on the secondary-side diode to power the load. The secondary current ( $I_{sec}$ ) begins to decrease linearly from the peak value to zero. When the secondary current decreases to zero, the primary-side leakage inductance, magnetizing inductance and all the parasitic capacitances decrease the MOSFET drain-source voltage—this decrease is also reflected on the auxiliary winding (see Figure 2). The zero-current detector in the ZCD pin generates the turn-on signal of the external MOSFET when the ZCD voltage falls below 0.31V (see Figure 3).

As a result, there are virtually no primary-switch turn-on losses and no secondary-diode reverse-recover losses. It ensures high efficiency and low EMI noise.



**Figure 2—Boundary Conduction Mode**



**Figure 3—Zero Current Detector**

### Real Current Control

The proprietary real-current control method allows the MP4021 to control the secondary-side LED current from primary-side information. The mean output LED current can be calculated approximately as:

$$I_o \approx \frac{N \cdot V_{FB}}{2 \cdot R_s}$$

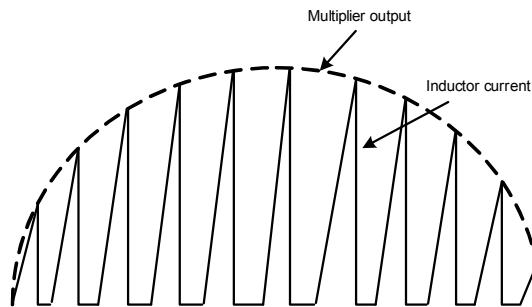
N—Turn ratio of primary side to secondary side

$V_{FB}$ —The feedback reference voltage (typical 0.4V)

$R_s$ —The sensing resistor connected between the MOSFET source and GND.

### Power Factor Correction

The MULT pin is connected to the tap of the resistor divider from the rectified instantaneous line voltage and fed as one input of the Multiplier. The output of the multiplier will be shaped as sinusoid too. This signal provides the reference for the current comparator and comparing with the primary side inductor current which sets the primary peak current shaped as sinusoid with the input line voltage. High power factor can be achieved.

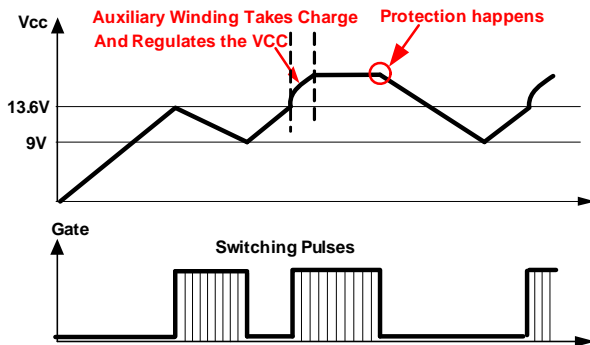


**Figure 4—Power Factor Correction Scheme**

The maximum voltage of the multiplier output to the current comparator is clamped to 2.5V to get a cycle-by-cycle current limitation.

### VCC Under-voltage Lockout

When the VCC voltage drops below UVLO threshold 9V, the MP4021 stops switching and totally shuts down, the VCC will restart charging by the external start up resistor from AC line. Figure 5 shows the typical waveform of VCC under-voltage lockout



**Figure 5—VCC Under-Voltage Lockout**

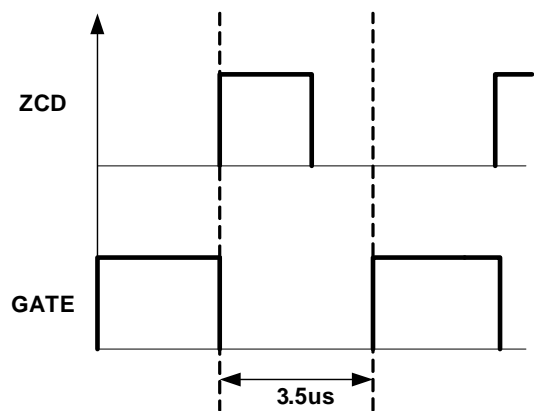
### Auto Starter

The MP4021 integrates an auto starter, the starter starts timing when the MOSFET is turned

off, if ZCD fails to send out another turn on signal after 130 $\mu$ s, the starter will automatically send out the turn on signal which can avoid the IC unnecessary shut down by ZCD missing detection.

### Minimum Off Time

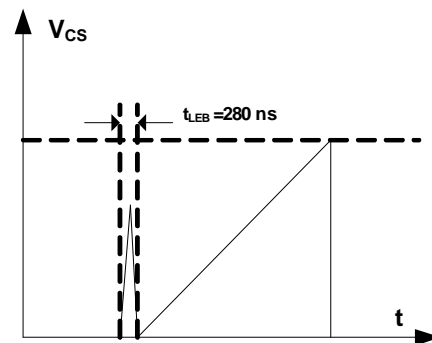
The MP4021 operates with variable switching frequency, the frequency is changing with the input instantaneous line voltage. To limit the maximum frequency and get a good EMI performance, MP4021 employs an internal minimum off time limiter—3.5 $\mu$ s, show as Figure 6.



**Figure 6—Minimum Off Time**

### Leading Edge Blanking

In order to avoid the premature termination of the switching pulse due to the parasitic capacitance discharging at MOSFET turning on, an internal leading edge blanking (LEB) unit is employed between the CS Pin and the current comparator input. During the blanking time, the path, CS Pin to the current comparator input, is blocked. Figure 7 shows the leading edge blanking.



**Figure 7—Leading Edge Blanking**

### Output Over-Voltage Protection (OVP)

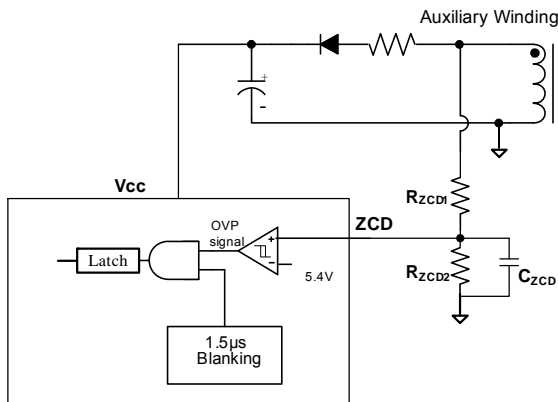
Output over voltage protection can prevent the components from damage in the over voltage condition. The positive plateau of auxiliary winding voltage is proportional to the output voltage, the OVP uses the auxiliary winding voltage instead of directly monitoring the output voltage, the OVP sample is shown in Figure 8. Once the ZCD pin voltage is higher than 5.4V, the OVP signal will be triggered and latched, the gate driver will be turned off and the IC work at quiescent mode, the VCC voltage dropped below the UVLO which will make the IC shut down and the system restarts again. The output OVP setting point can be calculated as:

$$V_{OUT\_OVP} \cdot \frac{N_{AUX}}{N_{SEC}} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = 5.4V$$

$V_{OUT\_OVP}$ —Output over voltage protection point

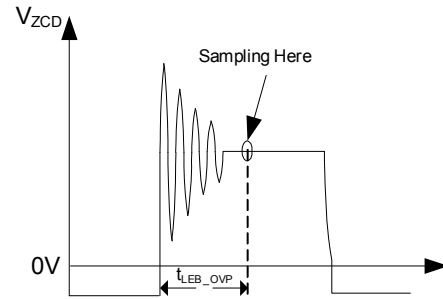
$N_{AUX}$ —The auxiliary winding turns

$N_{SEC}$ —The secondary winding turns



**Figure 8—OVP Sample Unit**

To avoid the mis-trigger OVP by the oscillation spike after the switch turns off, the OVP sampling has a  $t_{LEB\_OVP}$  blanking period, typical 1.5µs, shown in Figure 9.

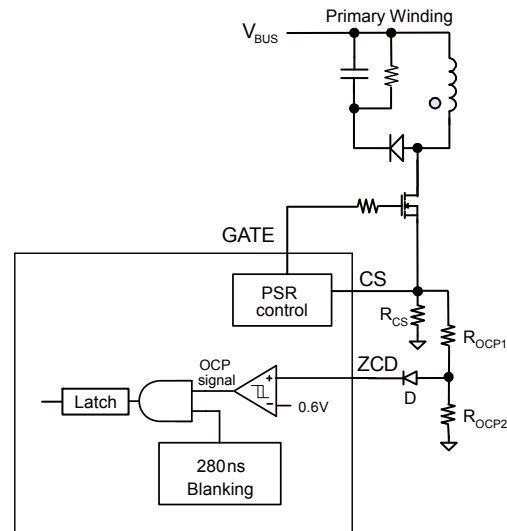


**Figure 9—ZCD Voltage and OVP Sample**

### Output Short Circuit Protection

The MP4021 clamps the CS pin voltage to less than 2.5V to limit the available output power. If the short circuit of the secondary-side occurs, the voltage of the auxiliary winding will fall down following the voltage of the secondary winding and the VCC drops to less than UV threshold and re-start the system.

As supplementary, tie a resistor divider from CS sensing resistor to ZCD pin, shown in Figure 10. When the power MOSFET in the primary-side is turned on, the ZCD pin monitors the rising primary-side current, once the ZCD pin reaches OCP threshold, typical 0.6V, the gate driver will be turned off to prevent the chip from damage and the IC works at quiescent mode, the VCC voltage dropped below the UVLO which will make the IC shut down and the system restarts again. Please note that the value of the resistors to set the OCP threshold ( $R_{OCP1}$  &  $R_{OCP2}$ ) should be much smaller than those of the ZCD zero-current detector ( $R_{ZCD1}$  &  $R_{ZCD2}$ )



**Figure 10—OCP Sample Unit**

The primary-side OCP setting point can be calculated as:

$$I_{PRI\_OCP} \cdot R_{CS} \cdot \frac{R_{OCP2}}{R_{OCP1} + R_{OCP2}} - V_D = 0.6V$$

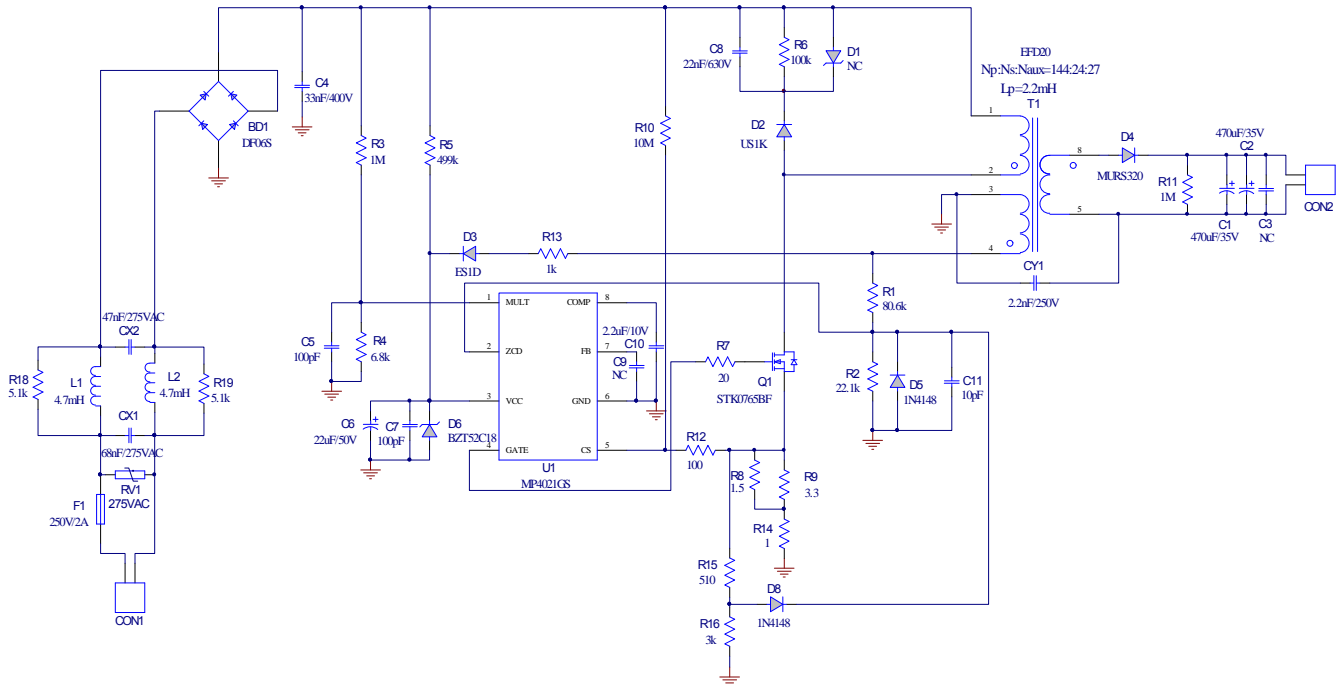
$I_{PRI\_OCP}$ —Primary-side over current protection point

### Thermal Shut Down

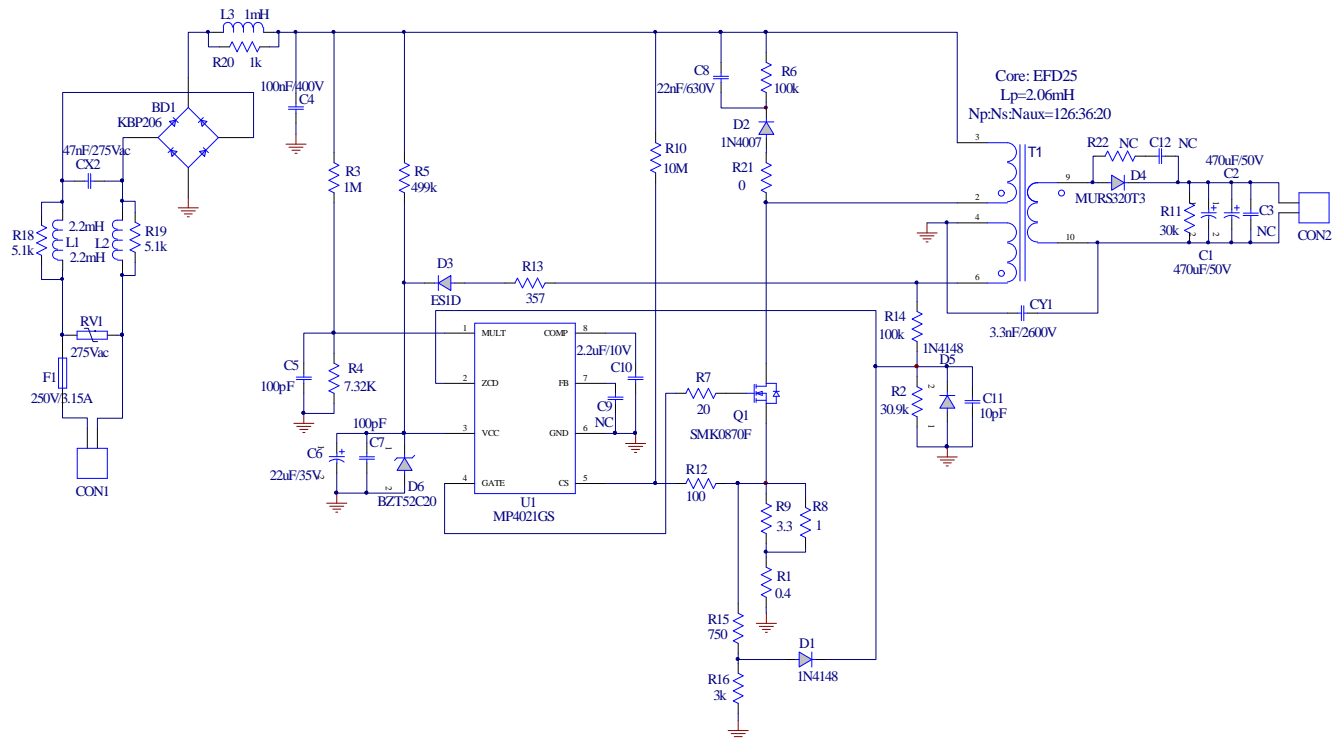
To prevent from any lethal thermal damage, when the inner temperature exceeds OTP threshold, the MP4021 shuts down switching cycle and latched until VCC drop below UVLO and restart again.

### Design Example

For the design example, please refer to MPS application note AN038 for the detailed design procedure and information.

**TYPICAL APPLICATION CIRCUIT**


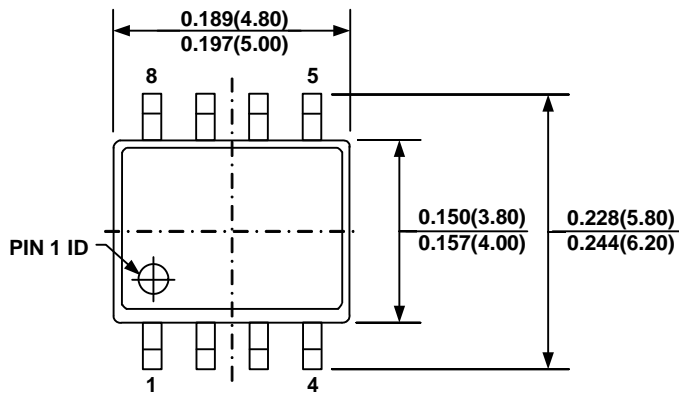
**Figure 11—Universal Input, Isolated Flyback Converter, Drive 5 LEDs in Series, 500mA LED Current for 8W LED Bulb Lighting**



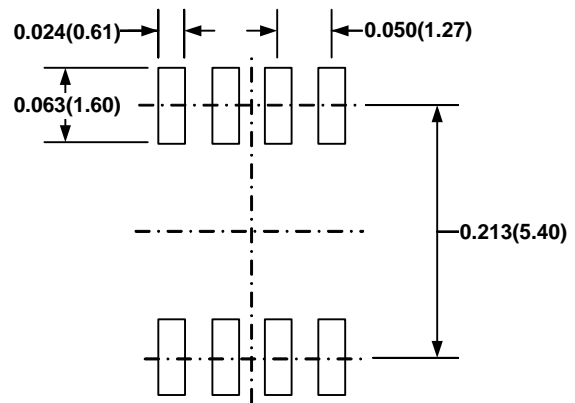
**Figure 12—Universal Input, Isolated Flyback Converter, Drive 9 LEDs in Series, 500mA LED Current for 15W LED Tube Lighting**

## PACKAGE INFORMATION

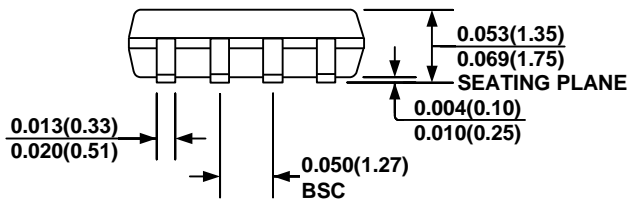
### SOIC8



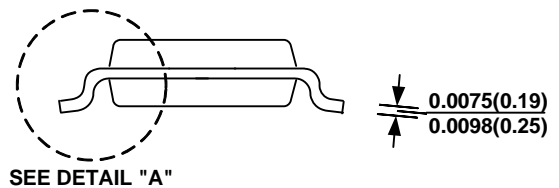
**TOP VIEW**



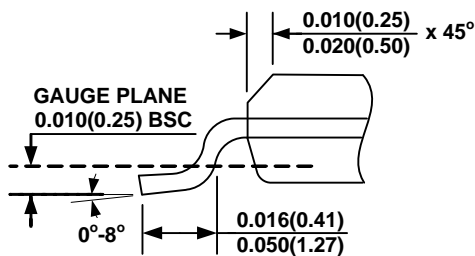
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**



**DETAIL "A"**

**NOTE:**

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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