AN1568/D

Interfacing Between LVDS and ECL

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APPLICATION NOTE

Introduction

Recent growth in high−speed data transmission between high−speed ICs demand more bandwidth than ever before while still maintaining high performance, low power consumption and good noise immunity. Emitter Coupled Logic (ECL) recognized the challenge and provided high performance and good noise immune devices. ECL migrated toward low voltages to reduce the power consumption and to keep up with current technology trends by offering 3.3 V and 2.5 V Low Voltage ECL (LVECL) devices.

LVDS (Low Voltage Differential Signaling) technology also addresses the needs of current high performance applications. LVDS as specified in ANSI/TIA/EIA−644 by Data Transmission Interface committee TR30.2 and IEEE 1596.3 SCI−LVDS by IEEE Scalable Coherent Interface standard (SCI) is a high speed, low power interface that is a solution in many application areas. LVDS provides an output swing of 250 mV to 400 mV with a DC offset of 1.2 V. External resistor components are required for board−to−board data transfer or clock distribution.

LVECL and LVDS are both differential voltage signals, but with different output amplitude and offset. The purpose of this documentation is to show the interfacing between LVECL and LVDS. In addition, it gives interface recommendations to and from 5.0 V supplied PECL devices and negative supplied ECL or NECL

ECL levels

Today's applications typically use ECL devices in the PECL mode. PECL (Positive ECL) is nothing more than supplying any ECL device with a positive power supply (V_{CC} = +5.0 V, V_{EE} = 0 V). In addition, ECL uses differential data transmission technology, which results in better noise immunity. Since the common mode noise is coupled onto the differential interconnect, it will be seen as a common mode modulation and will be rejected.

With the trend towards low voltage systems, a new generation of ECL circuitry has been developed. The Low Voltage NECL (LVNECL) devices work using negative –3.3 V or –2.5 V power supply, or more popular positive power supplies, V_{CC} = +3.3 V or +2.5 V and V_{EE} = GND as LVPECL. LVECL maintains 750 mV output swing with a 0.9 V offset from V_{CC}, which makes them ideal as peripheral components.

The temperature compensated (100EL, 100LVEL, 100EP, 100LVEP) output DC levels for the different supply levels are shown in Table 1. ECL outputs are designed as an open emitter, requiring a DC path to a more negative supply than V_{OL}. (see AND8020 for ECL Termination information).

ECL standard DC input levels are also relative to V_{CC}. Many devices are available with Voltage Input HIGH Common Mode Range (V_{IHCMR}). These differential inputs allow processing signals with small $V_{INPPMIN}$ (down to 200 mV, 150 mV or even 50 mV signal levels) within an appropriate offset range. The V_{IHCMR} ranges of ECL devices are listed in each respective data sheets.

Table 1. MC100EXXX/MC100ELXXX/LVELXXX/EPXXX/LVEPXXX (T_A = 0°C to +85°C)

Symbol	Parameter	2.5 V LVPECL (Note 1)	3.3 V LVPECL (Note 1)	5.0 V PECL (Note 1)	NECL	Unit
V_{CC}	Positive Supply Voltage	+2.5	+3.3	+5	GND	V
V_{EE}	Negative Supply Voltage	GND	GND	GND	−5.2, −4.5, −3.3 or −2.5	V
V_{OH}	Maximum Output HIGH Level	1.680	2.480	4.180	−0.820	V
V_{OH}	Typical Output HIGH Level	1.555	2.355	4.055	−0.945	V
V_{OH}	Minimum Output HIGH Level	1.430	2.230	3.930	−1.070	V
V_{OL}	Maximum Output LOW Level	0.880	1.680	3.380	−1.620	V
V_{OL}	Typical Output LOW Level	0.755	1.555	3.255	−1.745	V
V_{OL}	Minimum Output LOW Level	0.630	1.430	3.130	−1.870	V

1. All levels vary 1:1 with V_{CC} and loaded with 50 Ω to V_{CC} − 2.0 V.

LVDS Levels

As the name indicates, the LVDS main attribute is the low voltage amplitude levels compared to other data transmission standards, as shown in Figure 1. The LVDS specification states 250 mV to 400 mV output swing for driver/transmitter (V_{OUTPP}). The low voltage swing levels result in low power consumption while maintaining high performance levels required by most users. In addition, LVDS uses differential data transmission technology equivalent to ECL. Furthermore, LVDS technology is not dependent on specific power supply levels like ECL technology. This signifies an easy migration path to lower supply voltages such as 3.3 V, 2.5 V, or lower voltages while still maintaining the same signaling levels and high performance. ON Semiconductor currently provides a 2.5 V 1:5 dual differential LVDS Clock Driver/Receiver (MC100EP210S).

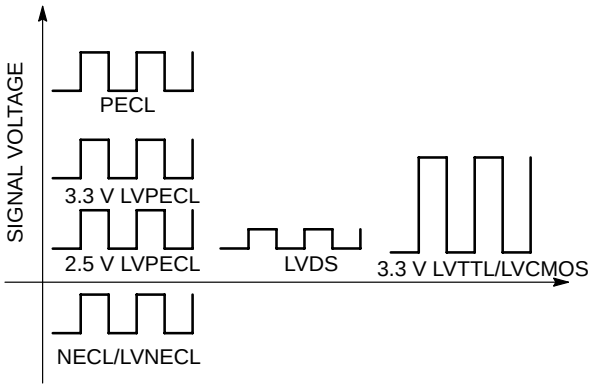

Figure 1. Comparison of Output Voltage Levels Standards (Figure not to Scale)

LVDS require a 100 Ω load resistor between the differential outputs to generate the Differential Output Voltage (V_{OD}) with a maximum current of 2.5 mA flowing through the load resistor. This load resistor will terminate the 50 Ω controlled characteristic impedance line, which prevent reflections and reduces unwanted electromagnetic emission (Figure 2).

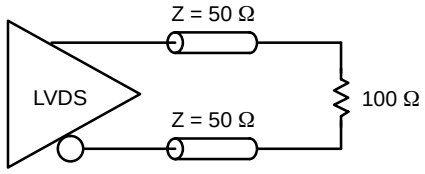

Figure 2. LVDS Output Definition

LVDS receivers require 200 mV minimum input swing within the input voltage range of 0 V to 2.4 V and can tolerate a minimum of ±1.0 V ground shift between the driver's ground and the receiver's ground, since LVDS receivers have a typical driver offset voltage of 1.2 V. The common mode range of the LVDS receiver is 0.2 V to 2.2 V, and the recommended LVDS receiver input voltage range is from 0 V to 2.4 V. Common mode range of LVDS is similar to the theory of Voltage Input HIGH Common Mode Range (V_{IHCMR}) of ECL devices.

Currently more LVDS standards are being developed as LVDS technology gains in popularity.

BLVDS

Bus LVDS (BLVDS) was developed for multipoint applications. This standard is targeted at heavily loaded back planes, which reduces the impedance of the transmission line by 50% or more. By providing increased drive current, the double termination seen by the driver will be compensated.

M−LVDS

TIA TR30.2 standards group is developing another multipoint LVDS application called Multipoint LVDS (M−LVDS). The maximum data rate is 500 Mbps.

GLVDS and SLVS

Ground referenced LVDS (GLVDS) is similar to LVDS except the driver output voltage offset is nearer to ground. The advantage of GLVDS is the use of very low power supply voltages (0.5 V).

Similar standard to GLVDS is SLVS (Scalable Low−Voltage Signaling for 400 mV) by JEDEC. The interface is terminated to ground with 400mV swing and a minimum supply voltage of 0.8 V.

LVDM

LVDM is designed for double 100 Ω−terminated applications. The driver's output current is two times the standard LVDS, thus producing LVDS characteristic levels.

Interfacing

Common mode range inputs are capable of processing signals with 150 mV to 400 mV amplitude. The ECL input processes signals up to 1.0 V amplitude. The DC voltage levels should be within the voltage input HIGH common mode range (V_{IHCMR}).

To interface between these two voltage levels, capacitive coupling can be used. Only clock or coded signals should be capacitively coupled. A capacitive coupling of NRZ signals will cause problems, which can require a passive or active interfacing.

Table 2. LVDS LEVELS

		LVDS Specification		BLVDS Specification		M−LVDS Specification		GLVDS Specification		LVDM Specification			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
Transmitter													
V_{PP}	Output Differential Voltage	250	400	240	500	480	650	150	500	247	454	mV	
V_{OS}	Output Offset Voltage	1125	1275	1225	1375	300	2100	75	250	1.125		mV	
R_L	Load Resistor	100		27	50	50		Internal To Rx		50		Ω	
I_{OD}	Output Differential Current	2.5	4.5	9	17	9	13	Adjustable		6		mA	
Receiver													
	Input Voltage Range	0	2400	0	2400	−1000	3800	−500	1000	0	2400	MV	V_{gpd} < 950 mV (Note 2)
	Differential HIGH Input Threshold		+100		+100		+50		+100		+100	mV	V_{gpd} < 950 mV (Note 2)
	Differential LOW Input Threshold	−100		−100		−50		−100		−100		mV	V_{gpd} < 950 mV (Note 2)

2. Vgpd is the voltage of Ground Potential Delta across or between boards.

Capacitive Coupling LVDS to ECL

Capacitive Coupling LVDS to ECL Using V_{BB}

Several ECL devices provide an externally accessible V_{BB} ($V_{BB} \approx V_{CC} -1.3V$) reference voltage. This ECL reference voltage can be used for differential capacitive coupling. The 10 nF capacitor can be used to decouple V_{BB} to GND. (Figure 3)

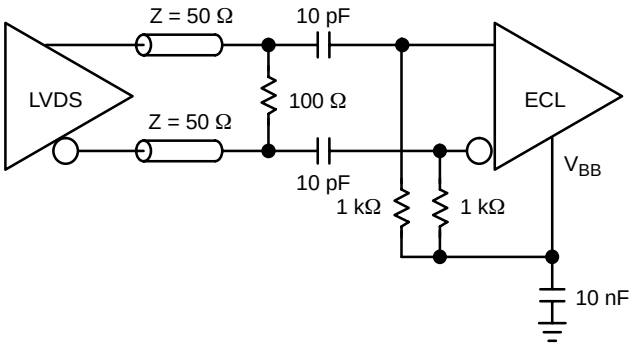

Figure 3. Capacitive Coupling LVDS to ECL Using V_{BB}

Capacitive Coupling LVDS to ECL with External Biasing

If V_{BB} reference voltage is not available, equivalent DC voltage can be generated using a resistor divider network. The resistor values depend on V_{CC} and V_{EE} voltages (Table 3). Stability is enhanced during null signal conditions if a 50 mV differential voltage is maintained between the divider networks. (Figure 4)

Table 3. Examples:

V_{CC} = GND	V_{EE} = −5.0 V	R1 = 1.2 kΩ	R2 = 3.4 kΩ
V_{CC} = GND	V_{EE} = −3.3 V	R1 = 680 Ω	R2 = 1.0 kΩ
V_{CC} = GND	V_{EE} = −2.5 V	R1 = 100 Ω	R2 = 90 Ω

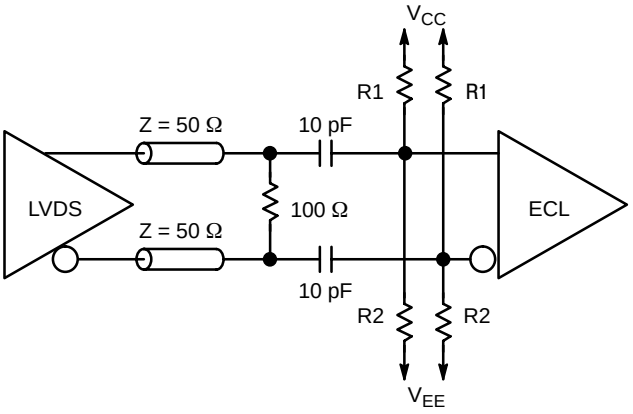

Figure 4. Capacitive Coupling LVDS to ECL with External Biasing

In the layout for both interfaces, the resistors and the capacitors should be located as close as possible to the ECL input to insure reduced reflection and increased signal integrity.

Capacitive Coupling ECL to LVDS

The ECL output requires a DC current path to V_{EE}; therefore, the pulldown termination resistors, R_T, are connected to V_{EE}. The Thevenin resistor pair represent the termination of the transmission line Z = R1 || R2 and generates an appropriate DC offset level of 1.2 V. (Figure 5)

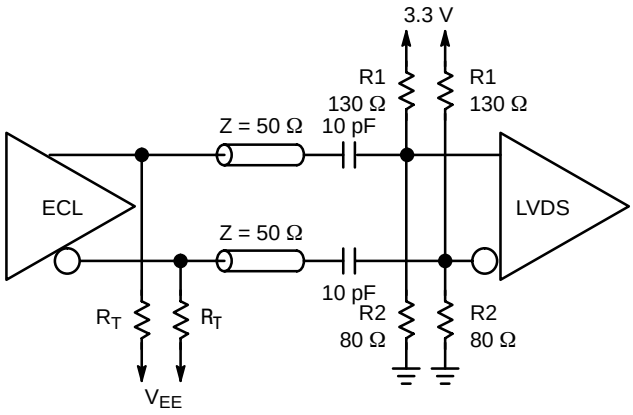

Figure 5. Capacitive Coupling ECL to LVDS

An example of capacitive coupled LVPECL (ECLinPS Plus™ Device) to LVDS is shown below. (Figure 6)

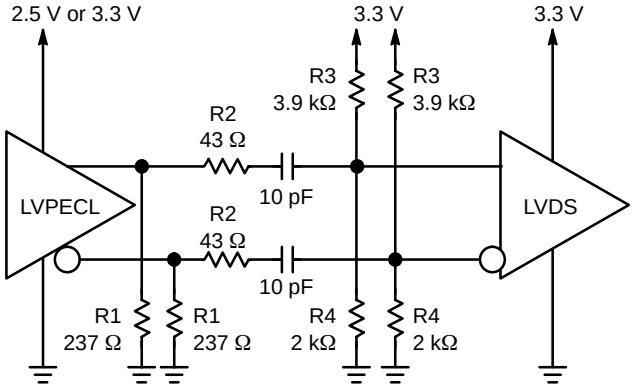

Figure 6. Capacitive Coupling LVPECL to LVDS

Capacitive Coupling ECL to LVDS Using V_{OS} Reference Voltage

Some LVDS devices supply external offset reference voltage (V_{OS}), which can be used for capacitive coupling. When the transmission line is very short, a parallel

termination should be used and placed as close as possible to the coupling capacitors. (Figure 7)

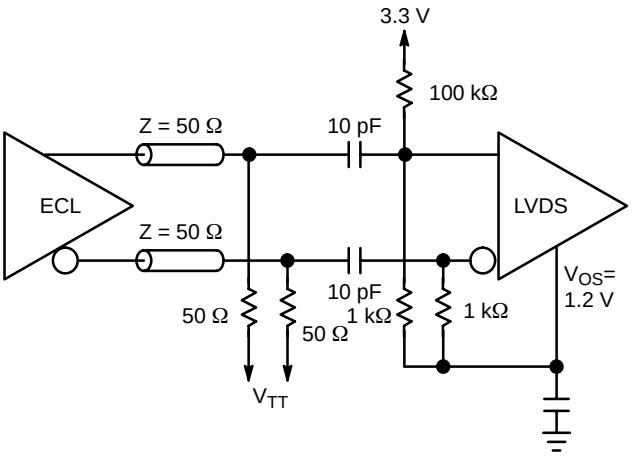

Figure 7. Capacitive Coupling ECL to LVDS Using V_{OS} Reference Voltage

Direct Interfacing

Interfacing from 2.5 V LVPECL to LVDS

Provided that the LVDS receiver can tolerate large input voltage peak to peak amplitude, 2.5 V LVPECL can be directly interfaced to LVDS receiver using proper ECL termination. 2.5 V LVPECL will be able to drive LVDS receiver with and without internal 100 Ω termination resistor. (See Figures 8, 9 and 10).

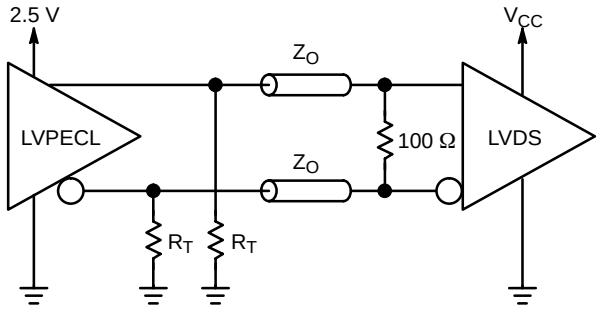

Figure 8. Interfacing 2.5 V LVPECL to LVDS with External 100 Ω Termination Resistor

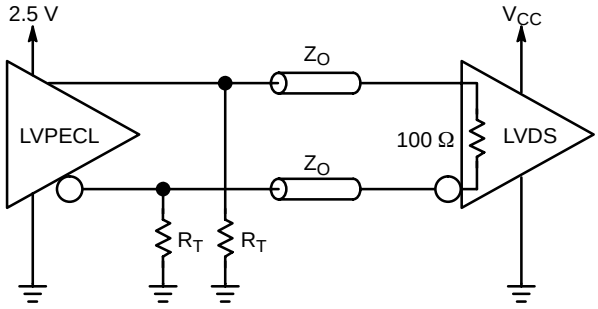

Figure 9. Interfacing 2.5 V LVPECL to LVDS with Internal 100 Ω Termination Resistor

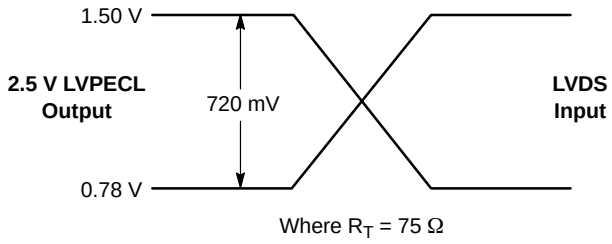

Figure 10. PSPICE Simulation Levels of 2.5V LVPECL to LVDS Interface with Example Resistor Values

Furthermore, sreies termination can be used to reduce the amplitude of the signal as described in AND8020 application note, by placing R_S resistor between the driver and the transmission line. (See Figures 11, 12 and 13).

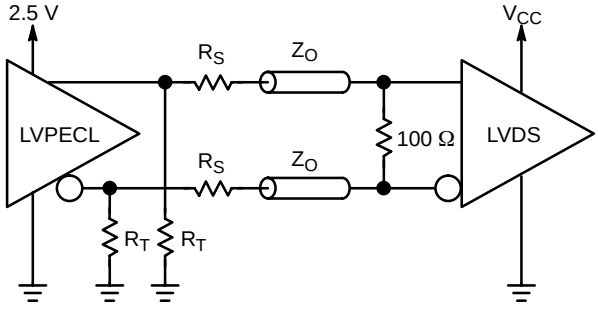

Figure 11. Interfacing 2.5 V LVPECL to LVDS with Series R_S and External 100 Ω Termination Resistor

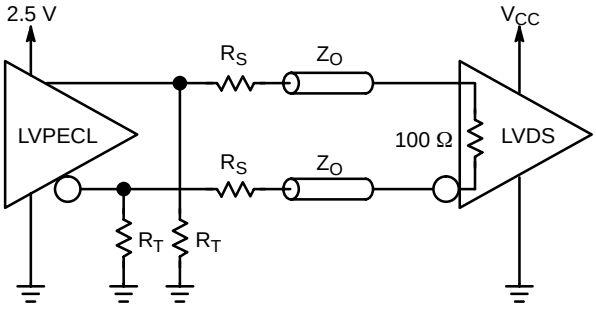

Figure 12. Interfacing 2.5 V LVPECL to LVDS with Series R_S and Internal 100 Ω Termination Resistor

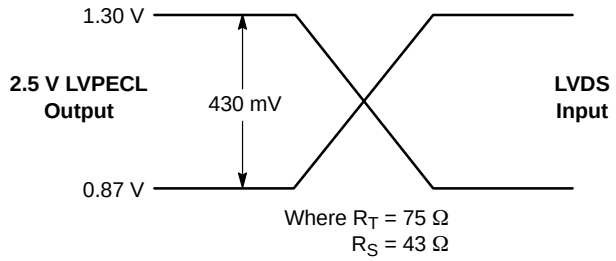

Figure 13. PSPICE Simulation Levels of 2.5V LVPECL to LVDS Interface with Series R_S Resistor

Interfacing from 3.3 V LVPECL to LVDS

Since the output levels V_{OH} and V_{OL} of 3.3 V LVPECL are more positive than the input range of LVDS receiver, special interface is required. (See Figures 14 and 15). Furthermore, the open emitter design of the ECL output structure need proper termination, which can be incorporated with the resistor divider network to generate a proper LVDS DC levels (eq. 1).

$$R_1 + R_2 = R_T \qquad \text{(eq. 1)}$$

The resistor divider network will divide the output common mode voltage of LVPECL (V_{CM}(LVPECL)) to input common mode voltage of LVDS (V_{CM}(LVDS)).

$$\frac{R_2}{R_1 + R_2} = \frac{V_{CM(LVDS)}}{V_{CM(LVPECL)}} \qquad \text{(eq. 2)}$$

Where:

R_T = Termination Resistor
V_{CM}(LVPECL) = Common Mode Voltage
V_{CM}(LVDS) = Common Mode Voltage

3.3 V LVPECL will be able to drive LVDS receiver with and without internal 100 Ω termination resistor. The above equations may give non−standard resistor values and when choosing resistors off the shelf, to avoid cutoff condition under worst−case scenario.

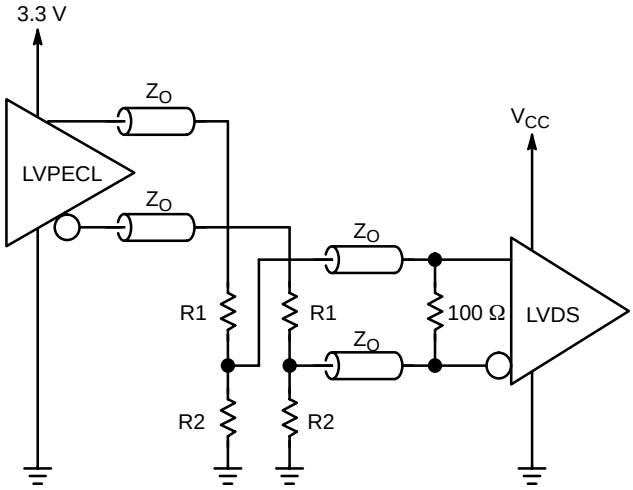

Figure 14. Interfacing 3.3 V LVPECL to LVDS

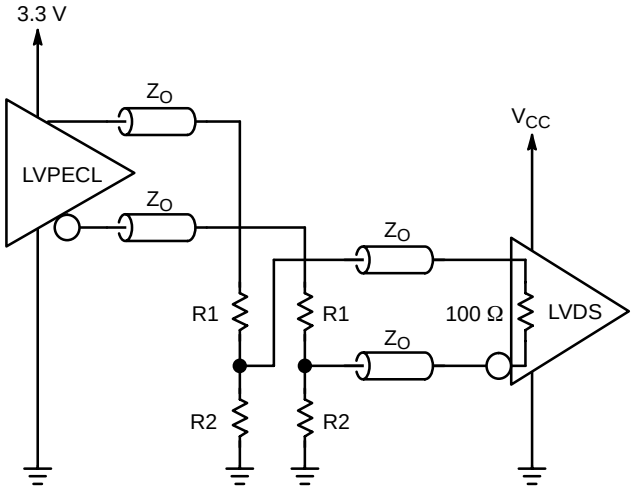

Figure 15. Interfacing LVPECL to LVDS with Internal 100 Ω Termination Resistor

Examples:

For 50 Ω controlled impedance, the resistor values for 3.3V LVPECL converted to LVDS voltage levels are as follows:

R_1 = 55 Ω
R_2 = 95 Ω
R_T = 150 Ω
V_{CM}(LVPECL) = 1.9 V
V_{CM}(LVDS) = 1.2 V

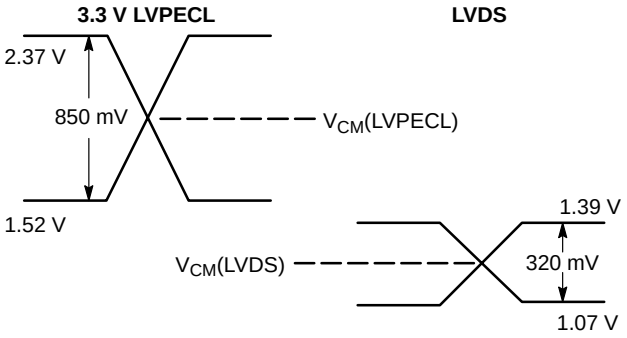

Figure 16. PSPICE Simulated Voltage Levels of 3.3 V LVPECL to LVDS Interface with Example Resistor Values

Interfacing from LVDS to LVPECL

The input common mode range of the low voltage ECL line receivers are wide enough to process LVDS signals. (Figure 17)

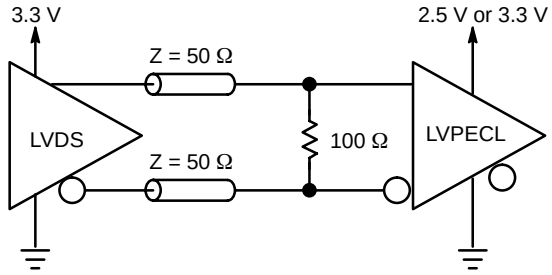

Figure 17. Interfacing LVDS to LVPECL

This direct interface is possible for all ECL devices with sufficiently low minimum differential input HIGH common mode range inputs. A differentially operated receiver's V_{IHCMR} minimum must be 1.2 V or less (see device data sheet).

Table 4. LVDS Input Compatible Devices

EP14	LVEP210S	LVEL37	EL56
EP809	LVE222	LVEL39	EL91
LVEP11	LVEL05	LVEL40	SG11
LVEP14	LVEL11	LVEL51	SG14
LVEP16	LVEL13	LVEL56	SG16
LVEP17	LVEL14	LVEL92	SG16M
LVEP34	LVEL16	EL13	SG16VS
LVEP56	LVEL17	EL14	SG53A
LVEP91	LVEL29	EL17	SG72A
LVEP111	LVEL32	EL29	SG86A
LVEP210	LVEL33	EL39	SG111

Interfacing from PECL to LVDS

Since the output levels V_{OH} and V_{OL} of 5 V PECL are more positive than the input range of LVDS receiver, special interface is required. (See Figure 18). Furthermore, the open emitter design of the ECL output structure need proper termination, which can be incorporated with the resistor divider network to generate a proper LVDS DC levels (eq. 3).

$$R_1 + R_2 = R_T \qquad \text{(eq. 3)}$$

The resistor divider network will divide the output common mode voltage of PECL (V_{CM}(PECL)) to input common mode voltage of LVDS (V_{CM}(LVDS)).

$$\frac{R_2}{R_1 + R_2} = \frac{V_{CM(LVDS)}}{V_{CM(PECL)}} \qquad \text{(eq. 4)}$$

Where:

R_T = Termination Resistor
V_{CM}(PECL) = Common Mode Voltage
V_{CM}(LVDS) = Common Mode Voltage

The above equations may give non—standard resistor values and when choosing resistors off the shelf, to avoid cutoff condition under worst−case scenario.

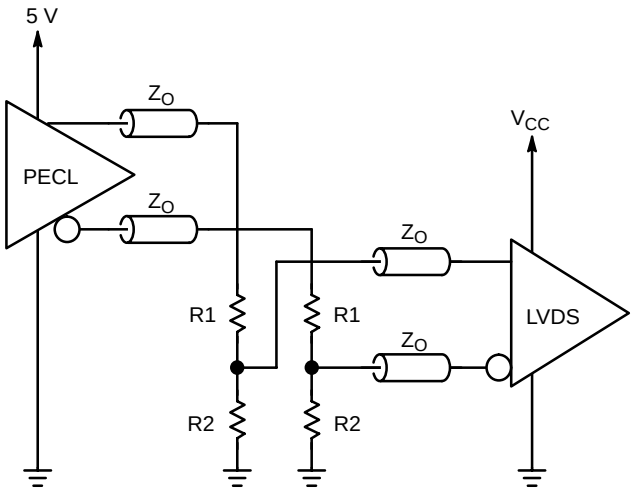

Figure 18. Interfacing 5 V PECL to LVDS

Examples:

For 50 Ω controlled impedance, the resistor values for 5V PECL converted to LVDS voltage levels are as follows:

R_1 = 134 Ω
R_2 = 66 Ω
R_T = 200 Ω
V_{CM}(PECL) = 3.65 V
V_{CM}(LVDS) = 1.2 V

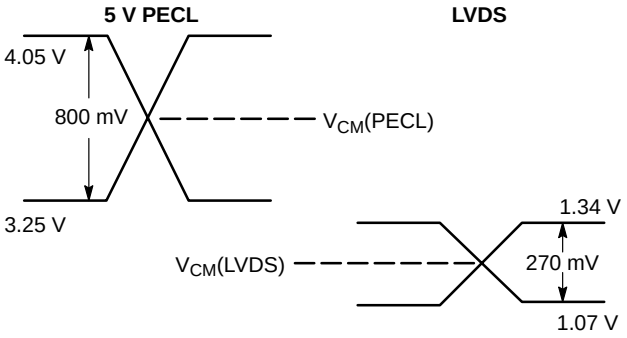

Figure 19. PSPICE Simulated Voltage Levels of 5 V PECL to LVDS Interface with Example Resistor Values

Interfacing from +3.3 V LVDS to +5.0 V PECL

To translate LVDS signals to PECL a differential ECL device with extended common mode range inputs (See Table 4) can be used to process and translate LVDS signals when supplied with 5.0 V ± 5% supply voltage. (See Figure 20)

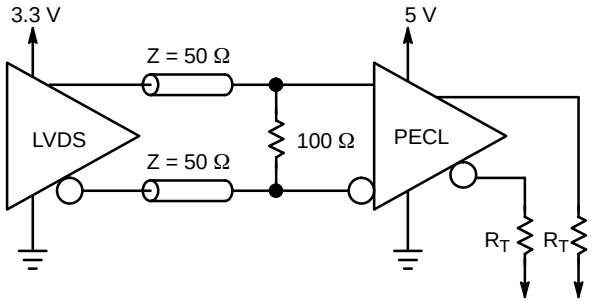

Figure 20. Interfacing LVDS to PECL

Interfacing Between NECL to LVDS

ON Semiconductor has developed level translators to interface between the different voltage levels. The MC100EP90 translates from negative supplied ECL to LVPECL. The interface from LVPECL to LVDS inputs is described above. (Figure 21)

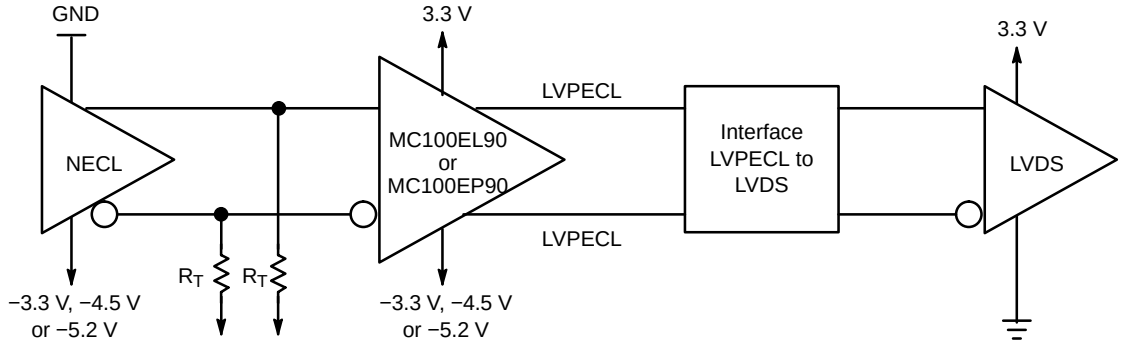

Figure 21. Interfacing from NECL to LVDS

To interface from LVDS to negative supplied ECL the common mode range (V_{IHCMR}) of the MC100LVEL91 for –3.3 V supply and the MC100EL91 for –4.5 V/–5.2 V supply is wide enough to process LVDS signals. (See Figure 22)

If V_{CC} = +5 V ± 5% supply and a V_{EE} = –5.2 V ± 5% supply is available the MC10E1651 can be used.

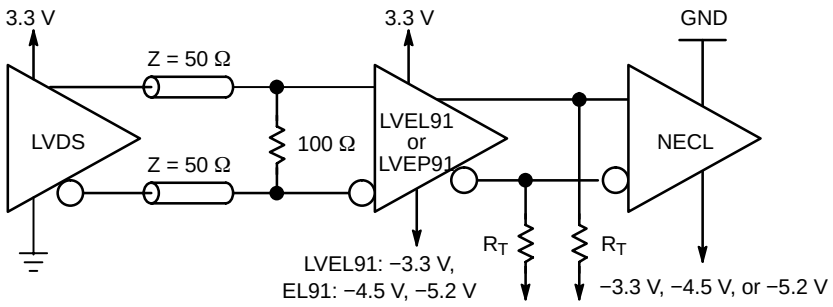

Figure 22. Interfacing from LVDS to NECL

Notes

ECLinPS Plus is a trademark of Semiconductor Components Industries, LLC (SCILLC).

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