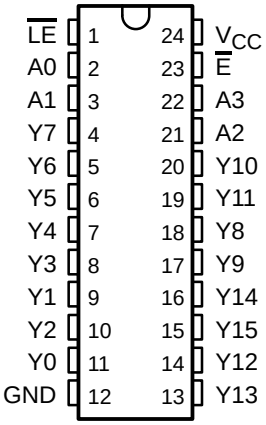
- **4.5-V to 5.5-V V_{CC} Operation Range**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . 10 LS-TTL Loads**
  - **Bus-Driver Outputs . . . 15 LS-TTL Loads**
- **Wide Operating Temperature Range of –55°C to 125°C**
- **Balanced Propagation Delays and Transition Times**
- **Significant Power Reduction Compared to LS-TTL Logic ICs**
- **HCT Types**
  - **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8 V (Max), V_{IH} = 2 V (Min)**
  - **CMOS Input Compatibility, $I_I \le 1\ \mu A$ at V_{OL}, V_{OH}**

E PACKAGE
(TOP VIEW)



description

The CD74HCT4514 and CD74HCT4515 are high-speed silicon-gate devices consisting of a 4-bit strobed latch and a 4-line to 16-line decoder. The selected output is enabled by a low on the enable ($\overline{E}$) input. A high on $\overline{E}$ inhibits selection of any output. Demultiplexing is accomplished by using $\overline{E}$ as the data input and the select inputs (A0–A3) as addresses. $\overline{E}$ also serves as a chip select when these devices are cascaded.

When the latch enable ($\overline{LE}$) is high, the output follows changes in the inputs (see decode function table). When $\overline{LE}$ is low, the output is isolated from changes in the input and remains at the level (high for the ’4514, low for the ’4515) it had before the latch was enabled.

To ensure the high-impedance state during power up or power down, $\overline{E}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74HCT4514E	CD74HCT4514E
			CD74HCT4515E	CD74HCT4515E

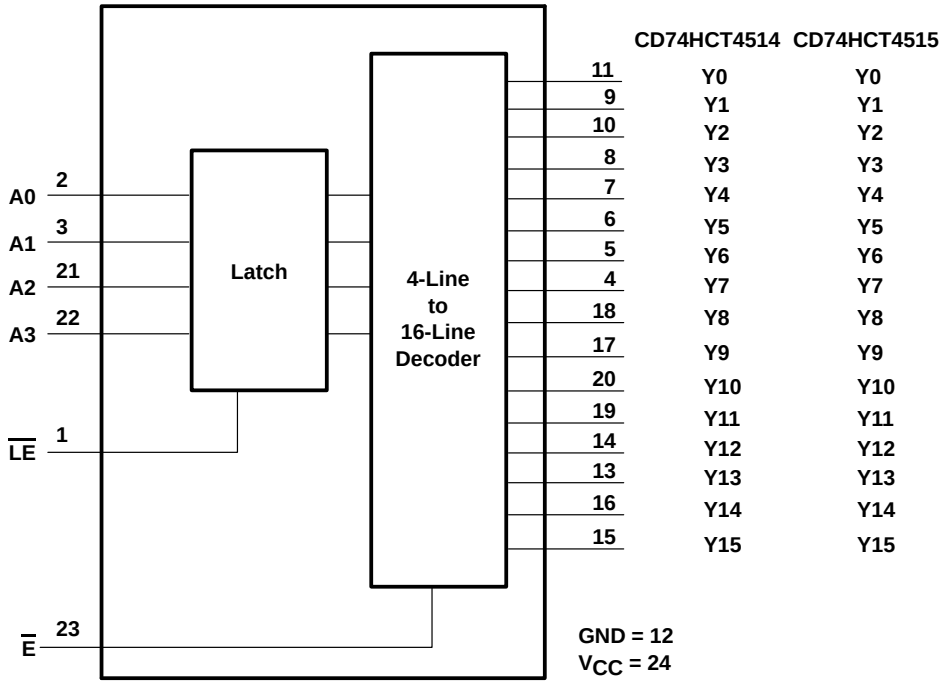
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DECODE FUNCTION TABLE
($\overline{LE}$ = H)

$\overline{E}$	DECODER INPUTS				ADDRESSED OUTPUT CD74HCT4514 = H CD74HCT4515 = L
	A3	A2	A1	A0	
L	L	L	L	L	Y0
L	L	L	L	H	Y1
L	L	L	H	L	Y2
L	L	L	H	H	Y3
L	L	H	L	L	Y4
L	L	H	L	H	Y5
L	L	H	H	L	Y6
L	L	H	H	H	Y7
L	H	L	L	L	Y8
L	H	L	L	H	Y9
L	H	L	H	L	Y10
L	H	L	H	H	Y11
L	H	H	L	L	Y12
L	H	H	L	H	Y13
L	H	H	H	L	Y14
L	H	H	H	H	Y15
H	X	X	X	X	All outputs = L, CD74HCT4514 All outputs = H, CD74HCT4515

H = high, L = low, X = don't care

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output drain current per output, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous output source or sink current per output, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 69°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 265°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		500	ns
T_A	Operating free-air temperature	–55	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	4.5 V	4.4		4.4		V
		I_{OH} = –6 mA		3.98		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	4.5 V		0.1		0.1	V
		I_{OL} = 6 mA			0.26		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	5.5 V		8		80	µA
ΔI_{CC}‡	One input at V_{CC} – 2.1 V,	Other inputs at 0 or V_{CC}	4.5 V to 5.5 V		360		450	µA
C_i					10		10	pF

‡ For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD
A0–A3	0.15
$\overline{LE}$	0.85
$\overline{E}$	0.3

Unit load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 360 μA max at 25°C).

timing requirements over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, $\overline{LE}$ high	30		38		ns
t_{su}	Setup time, data before $\overline{LE}\downarrow$	20		25		ns
t_h	Hold time, data after $\overline{LE}\downarrow$	5		5		ns

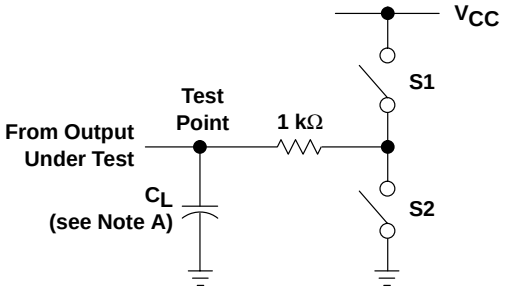
switching characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
t_{pd}	A0–A3	Y	C_L = 50 pF		55		69	ns
	$\overline{LE}$				50		63	
	$\overline{E}$				40		50	
t_t		Y	C_L = 50 pF		15		19	ns

operating characteristics, V_{CC} = 5 V, T_A = 25°C

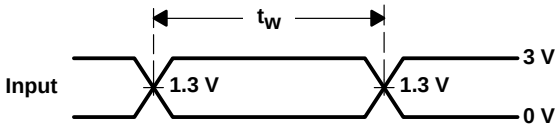
PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	75	pF

PARAMETER MEASUREMENT INFORMATION

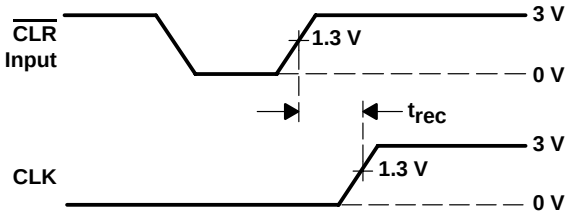


LOAD CIRCUIT

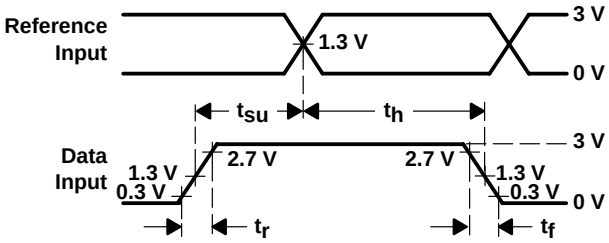
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



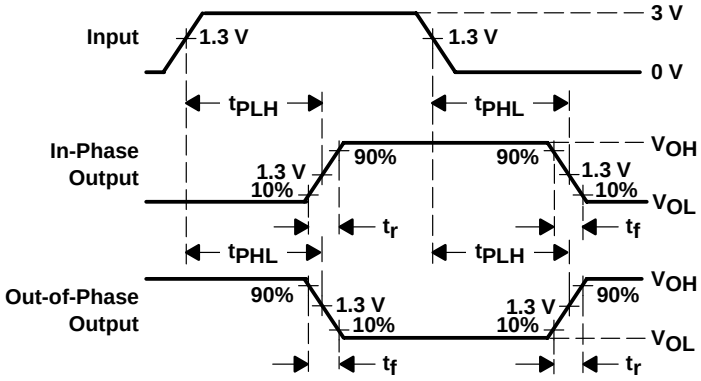
VOLTAGE WAVEFORMS
PULSE DURATION



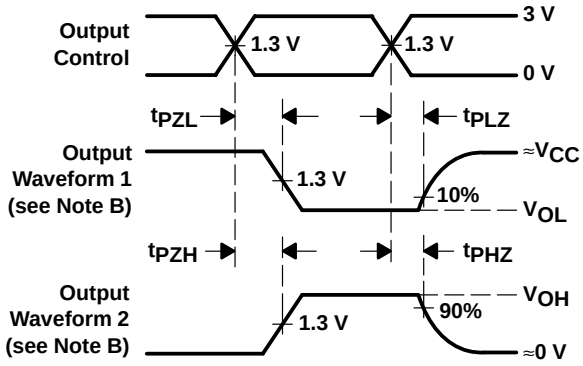
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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